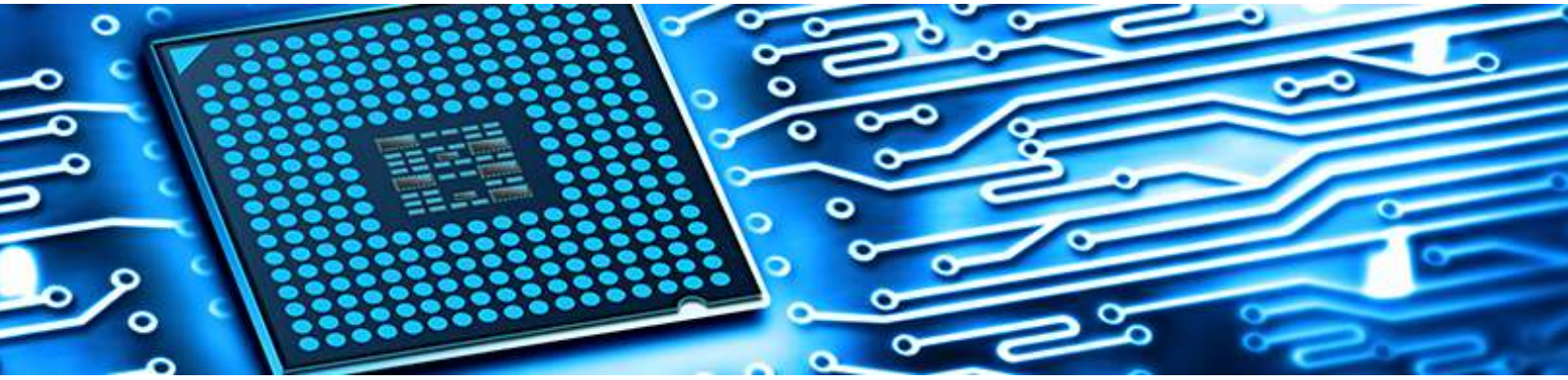

eNEX
Embedded & VLSI Training



Verilog

Introduction to Verilog HDL	Design and synthesis by using Verilog HDL Evolution of CAD Typical Design flow Importance of HDL's Popularity of Verilog HDL
Modeling Concepts	Design methodologies Module concept types of modeling
Basic Concepts	Lexical Conventions Number Specifications Strings Data Types System Task Compiler Directives
Modules	List of Ports Port Declaration Port Connection Pins
Gate Level Modeling	Different Types of Gates Gate Delays
Data Flow modeling	Continuous Assignments Delays Epression Operators Operators Types
Behavioural Modeling	Structured Procedures Initial Statement Always Statement Event- Base Timing Control Conditional Statements If Statements Case Statements Loop Statements
Task and Functions	Different between Task and Function Function Task
Switch Level Modeling(optional)	**Labs** • Introduction to XILINX tools • Entering HDL code • Synthesis and implementation • Creating Test Bench • Simulation

Course Duration:
Eligibility :
Course Fee :
Batch Size :